IN THE SPECIFICATION

Please replace the paragraph starting on page 9 with words " The n-type region 206..." with the following paragraph:

The n-type region 206 located between the source/drain extension 242 defines the channel region 250 of device 200. As shown in Figure 2, the source/drain regions are formed with a recess etch which creates a source/drain extension geometry which concaves inward creating an inflection point 260. The inflection point 260 is the location where the source/drain regions extend the greatest lateral distance beneath of gate electrode 202. In this way, when the recesses are back filled with highly conductive silicon or silicon alloy the distance between the source/drain extension regions is larger directly beneath the gate dielectric than is the distance deeper into the n-type region. That is, in accordance with an embodiment of the present invention source/drain regions are formed in a manner which creates a channel region 252 directly beneath the gate dielectric with a larger physical or metallurgical channel length (L_{met1}) than the physical or metallurgical channel length L_{met2} of the channel region 254 deeper into the substrate between the inflection points 260. Such a unique geometry provides improved performance in both the "on" and "off" states of the device. When the device is "off", the channel region remains n-type (no inversion). In the off condition any leakage (I_{off}) is due to holes traveling from the source/drain extension region to the other source/drain extension region directly beneath the gate oxide in region 252. In the off condition, holes experience a large channel length which greatly reduces the leakage current (i.e., reduces I_{off}) On the other hand, when device 200 is in the "ON" condition, n-type region 206 forms a channel by inverting the n-type silicon into p-type silicon. The inversion region forms a channel deeper into the substrate than the depth at which the inflection point 260 occurs. In this way, when the device is in the "on" condition and the inverted channel formed, a smaller L_{met2} is realized. A smaller L_{met2} during the "ON" state directly translates to a smaller channel resistance which results in a higher I_{on}.

Please replace the paragraph starting on page 16 with words " Yet another advantage of the lateral recess..." with the following paragraph:

Yet another advantage of the lateral recess etch process of the present invention is that the etch rate can be made slow, between 5-30Å per second, which causes the etch of the silicon substrate to concave inwards and from an inflection point 315 as shown in Figure 6. With this geometry, a large L_{met1} (metallurgical channel length or physical channel length) is achieved during the off state (low I_{off}) while a smaller L_{met2} is realized during the on state when the channels is formed. A smaller L_{met2} during the on state directly translates to a smaller channel resistance and enhance a higher I_{on}. Although a dry etch is preferred in the present invention a wet etch can also be used if desired.